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ACT-S512K32V High Speed 3.3Volt 16 Megabit SRAM Multichip Module

Features

- 4 Low Power CMOS 512K x 8 SRAMs in one MCM
- Overall configuration as 512K x 32
- Input and Output TTL Compatible
- 17, 20, 25, 35 & 45ns Access Times, 15ns Available by Special Order
- Full Military (-55°C to +125°C) Temperature Range
- +3.3V Power Supply
- Choice of Surface Mount or PGA Type Co-fired Packages:
  - 68–Lead, Dual-Cavity CQFP (F2), .88"SQ x .20"max (.18"max thickness available, contact factory for details) *(Drops into the 68 Lead JEDEC .99"SQ CQFJ footprint)*
  - 66–Pin, PGA-Type (P1), 1.38"SQ x .245"max
  - 66–Pin, PGA-Type (P7), 1.08"SQ x .185"max
- Internal Decoupling Capacitors
- DESC SMD# Pending

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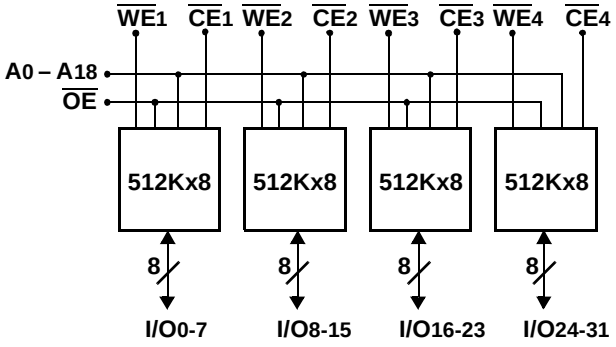
Block Diagram – PGA Type Package(P1,P7) & CQFP(F2)



Pin Description

I/O0-31	Data I/O
A0–18	Address Inputs
$\overline{WE}$1–4	Write Enables
$\overline{CE}$1–4	Chip Enables
$\overline{OE}$	Output Enable
Vcc	Power Supply
GND	Ground
NC	Not Connected

General Description

The ACT–S512K32V is a High Speed 4 megabit CMOS SRAM Multichip Module (MCM) designed for full temperature range, 3.3V Power Supply, military, space, or high reliability mass memory and fast cache applications.

The MCM can be organized as a 512K x 32 bits, 1M x 16 bits or 2M x 8 bits device and is input and output TTL compatible. Writing is executed when the write enable ($\overline{WE}$) and chip enable ($\overline{CE}$) inputs are low. Reading is accomplished when $\overline{WE}$ is high and $\overline{CE}$ and output enable ($\overline{OE}$) are both low. Access time grades of 17ns, 20ns, 25ns, 35ns and 45ns maximum are standard.

The products are designed for operation over the temperature range of -55°C to +125°C and screened under the full military environment. DESC Standard Military Drawing (SMD) part numbers are pending.

The ACT-S512K32V is manufactured in Aeroflex's 80,000ft^2 MIL-PRF-38534 certified facility in Plainview, N.Y.

Absolute Maximum Ratings

Symbol	Rating		Range	Units
T_C	Case Operating Temperature	Speed 15ns	-40 to +85	°C
		Speed 17ns to 45ns	-55 to +125	°C
T_{STG}	Storage Temperature		-65 to +150	°C
P_D	Maximum Package Power Dissipation			
	P1,P7 Package		3.0	W
	F2 Package		2.7	W
$Ø_{J-C}$	Hottest Die, Max Thermal Resistance - Junction to Case			
	P1,P7 Package		2.0	°C/W
	F2 Package		8.0	°C/W
V_G	Maximum Signal Voltage to Ground		-0.5 to +4.6	V
T_L	Maximum Lead Temperature (10 seconds)		300	°C

Normal Operating Conditions

Symbol	Parameter	Minimum	Maximum	Units
V_{CC}	Power Supply Voltage	+3.0	+3.6	V
V_{IH}	Input High Voltage	+2.0	V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	-0.3	+0.8	V

Capacitance

(f = 1MHz, T_C = 25°C)

Symbol	Parameter	Maximum	Units
C_{AD}	A_0 – A_{18} Capacitance	50	pF
C_{OE}	$\overline{OE}$ Capacitance	50	pF
C_{WE}	Write Enable Capacitance	20	pF
C_{CE}	Chip Enable Capacitance	20	pF
$C_{I/O}$	I/O_0 – I/O_{31} Capacitance	20	pF

Capacitance is guaranteed by design but not tested.

DC Characteristics

(3.0Vdc≤ V_{CC} ≤ 3.6Vdc, V_{SS} = 0V, T_C = -55°C to +125°C, Unless otherwise specified)

Parameter	Sym	Conditions	ALL Speeds Min	ALL Speeds Max	Units
Input Leakage Current	I_{LI}	V_{CC} = Max, V_{IN} = 0 or V_{CC}		10	µA
Output Leakage Current	I_{LO}	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IH}, V_{OUT} = 0 or V_{CC}		10	µA
Operating Supply Current 32 Bit Mode	I_{CC1}x32	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}, f = 5 MHz, V_{CC} = Max, CMOS Compatible		600	mA
Standby Current	I_{SB1}	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IH}, f = 5 MHz, V_{CC} = Max, CMOS Compatible		80	mA
Operating Supply Current 32 Bit Mode	I_{CC2}x32	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}, f = 50 MHz, V_{CC} = Max, CMOS Compatible		750	mA
Standby Current	I_{SB2}	$\overline{CE}$ = V_{CC}, $\overline{OE}$ = V_{IH}, f = 50 MHz, V_{CC} = Max, CMOS Compatible		240	mA
Output Low Voltage	V_{OL}	I_{OL} = 8 mA, V_{CC} = Min		0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0 mA, V_{CC} = Min	2.4		V

AC Characteristics

(V_{CC} = 3.3V, V_{SS} = 0V, Tc = -55°C to +125°C)

Read Cycle

Parameter	Sym	–017		–020		–025		–035		–045		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	17		20		25		35		45		ns
Address Access Time	t_{AA}		17		20		25		35		45	ns
Chip Enable Access Time	t_{ACS}		17		20		25		35		45	ns
Output Hold from Address Change	t_{OH}	0		0		0		0		0		ns
Output Enable to Output Valid	t_{OE}		9		10		12		25		35	ns
Chip Enable to Output in Low Z *	t_{CLZ}	3		3		3		3		3		ns
Output Enable to Output in Low Z *	t_{OLZ}	0		0		0		0		0		ns
Chip Deselect to Output in High Z *	t_{CHZ}		8		8		10		15		15	ns
Output Disable to Output in High Z *	t_{OHZ}		8		8		10		15		15	ns

* Parameters guaranteed by design but not tested

Write Cycle

Parameter	Sym	–017		–020		–025		–035		–045		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	17		20		25		35		45		ns
Chip Enable to End of Write	t_{CW}	15		15		20		30		35		ns
Address Valid to End of Write	t_{AW}	15		15		20		30		35		ns
Data Valid to End of Write	t_{DW}	12		12		15		20		30		ns
Write Pulse Width	t_{WP}	13		13		15		25		35		ns
Address Setup Time	t_{AS}	0		0		0		0		0		ns
Output Active from End of Write *	t_{OW}	0		0		0		0		0		ns
Write to Output in High Z *	t_{WHZ}		8		11		13		15		15	ns
Data Hold from Write Time	t_{DH}	0		0		0		0		0		ns
Address Hold Time	t_{AH}	0		1		2		2		2		ns

* Parameters guaranteed by design but not tested

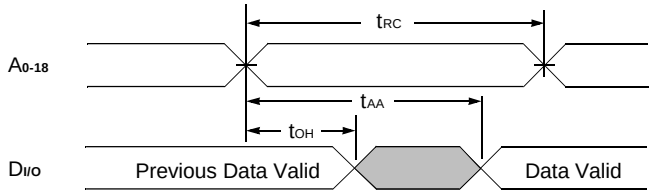
Truth Table

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Data I/O	Power
Standby	H	X	X	High Z	Standby (deselect/power down)
Read	L	L	H	Data Out	Active
Read	L	H	H	High Z	Active (deselected)
Write	L	X	L	Data In	Active

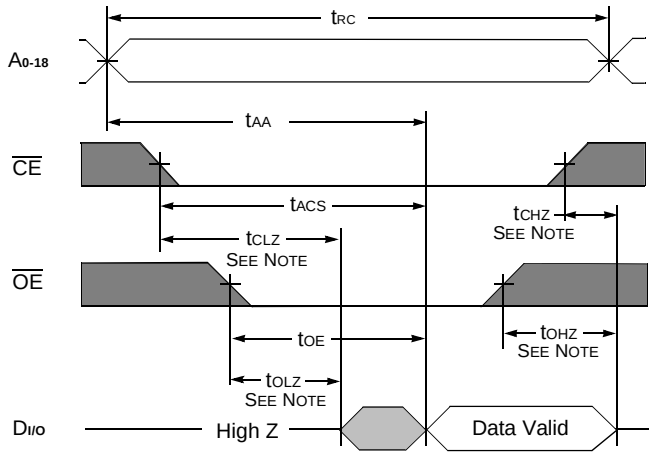
Timing Diagrams

Read Cycle Timing Diagrams

Read Cycle 1 ($\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH})



Read Cycle 2 ($\overline{WE}$ = V_{IH})



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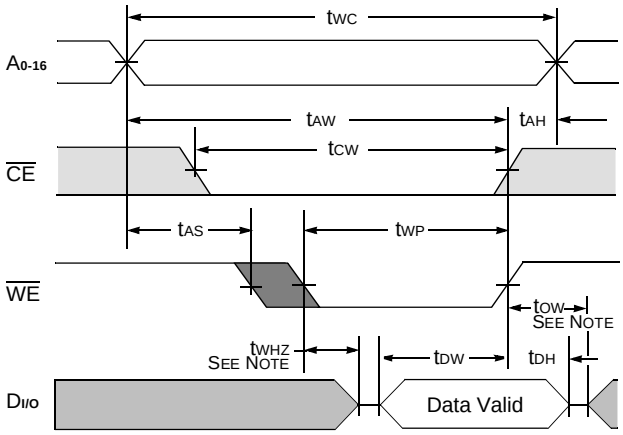
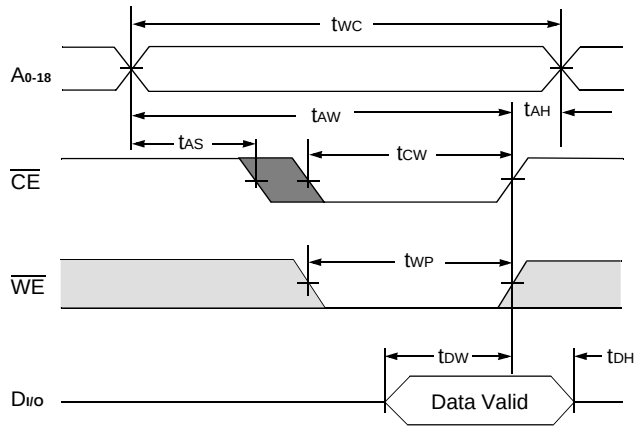
Write Cycle Timing Diagrams

Write Cycle 1 ($\overline{WE}$ Controlled, $\overline{OE}$ = V_{IL})

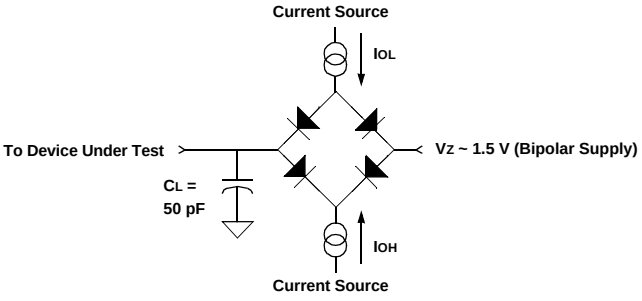


Write Cycle 2 ($\overline{CE}$ Controlled, $\overline{OE}$ = V_{IH})



Note: Guaranteed by design, but not tested.

AC Test Circuit



Parameter	Typical	Units
Input Pulse Level	0 – 3.0	V
Input Rise and Fall	5	ns
Input and Output Timing Reference Level	1.5	V

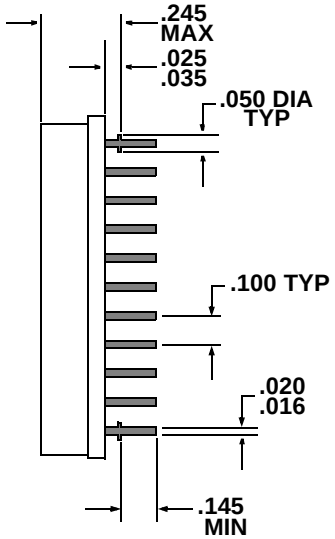
Notes:
1) V_Z is programmable from -2V to +4.6V. 2) I_{OL} and I_{OH} programmable from 0 to 16 mA. 3) Tester Impedance Z_O = 75Ω. 4) V_Z is typically the midpoint of V_{OH} and V_{OL}. 5) I_{OL} and I_{OH} are adjusted to simulate a typical resistance load circuit. 6) ATE Tester includes jig capacitance.

Pin Numbers & Functions

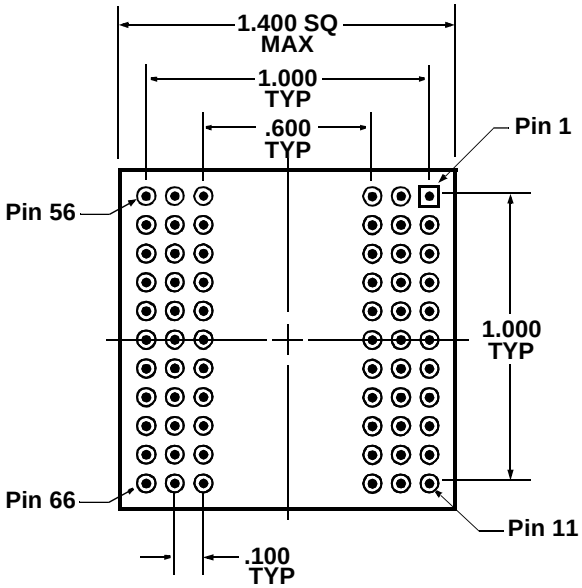
66 Pins — PGA-Type							
Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function
1	I/O_8	18	A_{12}	35	I/O_{25}	52	$\overline{WE}_3$
2	I/O_9	19	V_{CC}	36	I/O_{26}	53	$\overline{CS}_3$
3	I/O_{10}	20	$\overline{CS}_1$	37	A_6	54	GND
4	A_{13}	21	NC	38	A_7	55	I/O_{19}
5	A_{14}	22	I/O_3	39	NC	56	I/O_{31}
6	A_{15}	23	I/O_{15}	40	A_8	57	I/O_{30}
7	A_{16}	24	I/O_{14}	41	A_9	58	I/O_{29}
8	A_{17}	25	I/O_{13}	42	I/O_{16}	59	I/O_{28}
9	I/O_0	26	I/O_{12}	43	I/O_{17}	60	A_0
10	I/O_1	27	$\overline{OE}$	44	I/O_{18}	61	A_1
11	I/O_2	28	A_{18}	45	V_{CC}	62	A_2
12	$\overline{WE}_2$	29	$\overline{WE}_1$	46	$\overline{CS}_4$	63	I/O_{23}
13	$\overline{CS}_2$	30	I/O_7	47	$\overline{WE}_4$	64	I/O_{22}
14	GND	31	I/O_6	48	I/O_{27}	65	I/O_{21}
15	I/O_{11}	32	I/O_5	49	A_3	66	I/O_{20}
16	A_{10}	33	I/O_4	50	A_4		
17	A_{11}	34	I/O_{24}	51	A_5		

"P1" — 1.40" SQ PGA Type Package

Side View



Bottom View

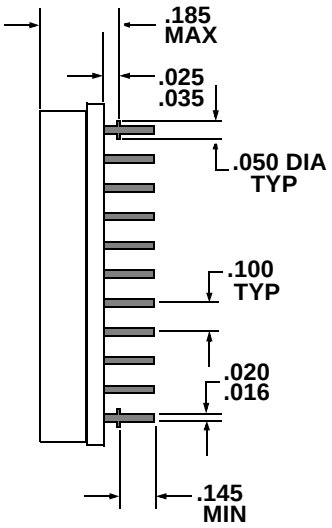


Pin Numbers & Functions

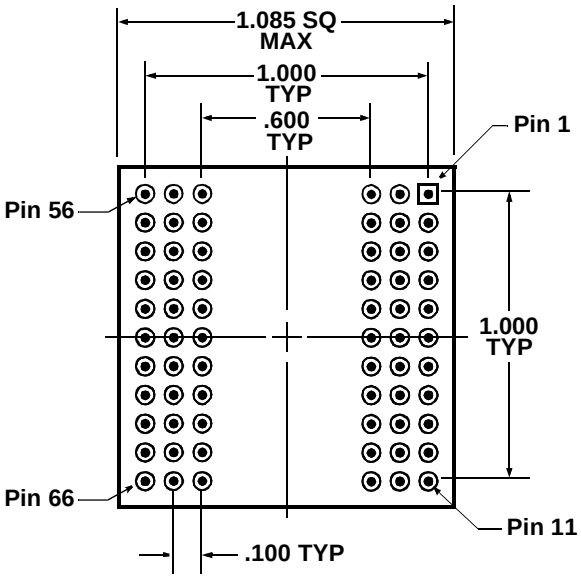
66 Pins — PGA-Type							
Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function
1	I/O_8	18	A_{12}	35	I/O_{25}	52	$\overline{WE}_3$
2	I/O_9	19	Vcc	36	I/O_{26}	53	$\overline{CE}_3$
3	I/O_{10}	20	$\overline{CE}_1$	37	A_6	54	GND
4	A_{13}	21	NC	38	A_7	55	I/O_{19}
5	A_{14}	22	I/O_3	39	NC	56	I/O_{31}
6	A_{15}	23	I/O_{15}	40	A_8	57	I/O_{30}
7	A_{16}	24	I/O_{14}	41	A_9	58	I/O_{29}
8	A_{17}	25	I/O_{13}	42	I/O_{16}	59	I/O_{28}
9	I/O_0	26	I/O_{12}	43	I/O_{17}	60	A_0
10	I/O_1	27	$\overline{OE}$	44	I/O_{18}	61	A_1
11	I/O_2	28	A_{18}	45	V_{CC}	62	A_2
12	$\overline{WE}_2$	29	$\overline{WE}_1$	46	$\overline{CE}_4$	63	I/O_{23}
13	$\overline{CE}_2$	30	I/O_7	47	$\overline{WE}_4$	64	I/O_{22}
14	GND	31	I/O_6	48	I/O_{27}	65	I/O_{21}
15	I/O_{11}	32	I/O_5	49	A_3	66	I/O_{20}
16	A_{10}	33	I/O_4	50	A_4		
17	A_{11}	34	I/O_{24}	51	A_5		

"P7" — 1.08" SQ PGA Type Package

Side View



Bottom View



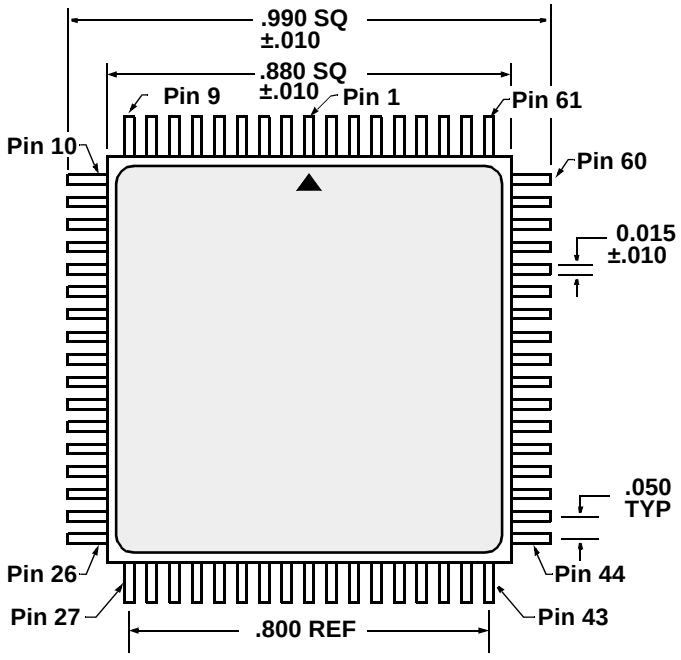
All dimensions in inches

Pin Numbers & Functions

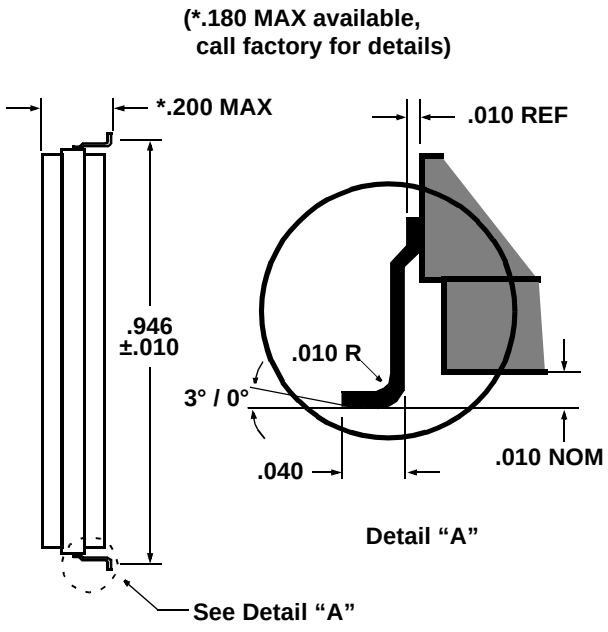
68 Pins — Dual-Cavity CQFP							
Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function
1	GND	18	GND	35	$\overline{OE}$	52	GND
2	$\overline{CE}_3$	19	I/O_8	36	$\overline{CE}_2$	53	I/O_{23}
3	A_5	20	I/O_9	37	A_{17}	54	I/O_{22}
4	A_4	21	I/O_{10}	38	$\overline{WE}_2$	55	I/O_{21}
5	A_3	22	I/O_{11}	39	$\overline{WE}_3$	56	I/O_{20}
6	A_2	23	I/O_{12}	40	$\overline{WE}_4$	57	I/O_{19}
7	A_1	24	I/O_{13}	41	A_{18}	58	I/O_{18}
8	A_0	25	I/O_{14}	42	NC	59	I/O_{17}
9	NC	26	I/O_{15}	43	NC	60	I/O_{16}
10	I/O_0	27	V_{CC}	44	I/O_{31}	61	V_{CC}
11	I/O_1	28	A_{11}	45	I/O_{30}	62	A_{10}
12	I/O_2	29	A_{12}	46	I/O_{29}	63	A_9
13	I/O_3	30	A_{13}	47	I/O_{28}	64	A_8
14	I/O_4	31	A_{14}	48	I/O_{27}	65	A_7
15	I/O_5	32	A_{15}	49	I/O_{26}	66	A_6
16	I/O_6	33	A_{16}	50	I/O_{25}	67	$\overline{WE1}$
17	I/O_7	34	$\overline{CE}_1$	51	I/O_{24}	68	$\overline{CE}_4$

Package Outline "F2" — Dual-Cavity CQFP

Top View



All dimensions in inches



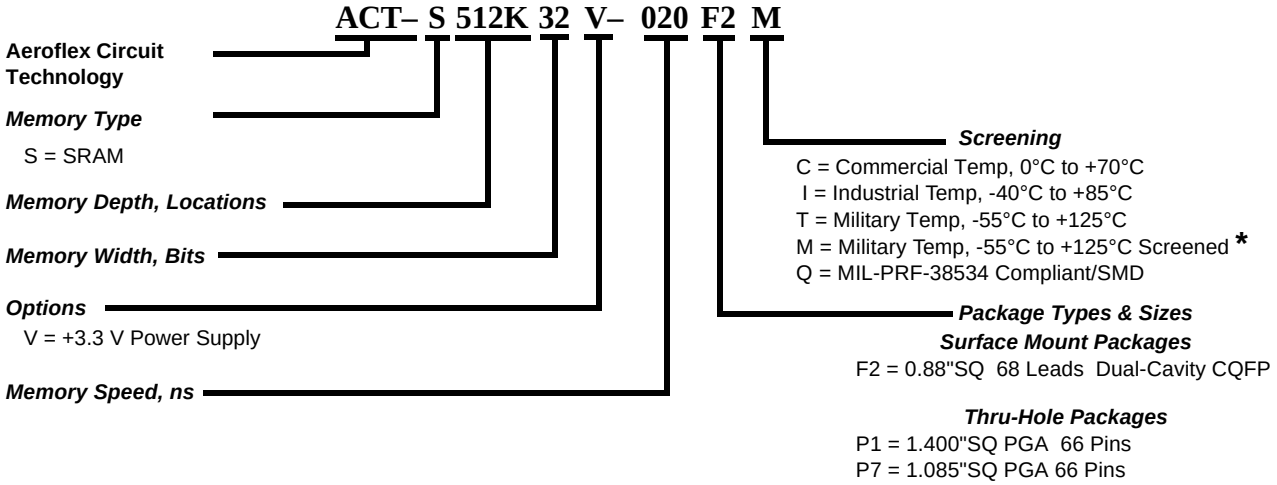
Note: Metallic lids and walls – both sides

AEROFLEX CIRCUIT TECHNOLOGY

Ordering Information

Model Number	DESC Part Number	Speed	Package
ACT–S512K32V–017F2Q	(Pending)	17ns	.88"sq CQFP
ACT–S512K32V–020F2Q	(Pending)	20ns	.88"sq CQFP
ACT–S512K32V–025F2Q	(Pending)	25ns	.88"sq CQFP
ACT–S512K32V–035F2Q	(Pending)	35ns	.88"sq CQFP
ACT–S512K32V–045F2Q	(Pending)	45ns	.88"sq CQFP
ACT–S512K32V–017P1Q	(Pending)	17ns	1.38"sq PGA-Type
ACT–S512K32V–020P1Q	(Pending)	20ns	1.38"sq PGA-Type
ACT–S512K32V–025P1Q	(Pending)	25ns	1.38"sq PGA-Type
ACT–S512K32V–035P1Q	(Pending)	35ns	1.38"sq PGA-Type
ACT–S512K32V–045P1Q	(Pending)	45ns	1.38"sq PGA-Type
ACT–S512K32V–017P7Q	(Pending)	17ns	1.08"sq PGA-Type
ACT–S512K32V–020P7Q	(Pending)	20ns	1.08"sq PGA-Type
ACT–S512K32V–025P7Q	(Pending)	25ns	1.08"sq PGA-Type
ACT–S512K32V–035P7Q	(Pending)	35ns	1.08"sq PGA-Type
ACT–S512K32V–045P7Q	(Pending)	45ns	1.08"sq PGA-Type

Part Number Breakdown


ACT– S 512K 32 V– 020 F2 M
Aeroflex Circuit Technology
Memory Type
S = SRAM
Memory Depth, Locations
Memory Width, Bits
Options
V = +3.3 V Power Supply
Memory Speed, ns
Screening
C = Commercial Temp, 0°C to +70°C
I = Industrial Temp, -40°C to +85°C
T = Military Temp, -55°C to +125°C
M = Military Temp, -55°C to +125°C Screened *
Q = MIL-PRF-38534 Compliant/SMD
Package Types & Sizes
Surface Mount Packages
F2 = 0.88"SQ 68 Leads Dual-Cavity CQFP
Thru-Hole Packages
P1 = 1.400"SQ PGA 66 Pins
P7 = 1.085"SQ PGA 66 Pins

* Screened to the individual test methods of MIL-STD-883

Specifications subject to change without notice

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